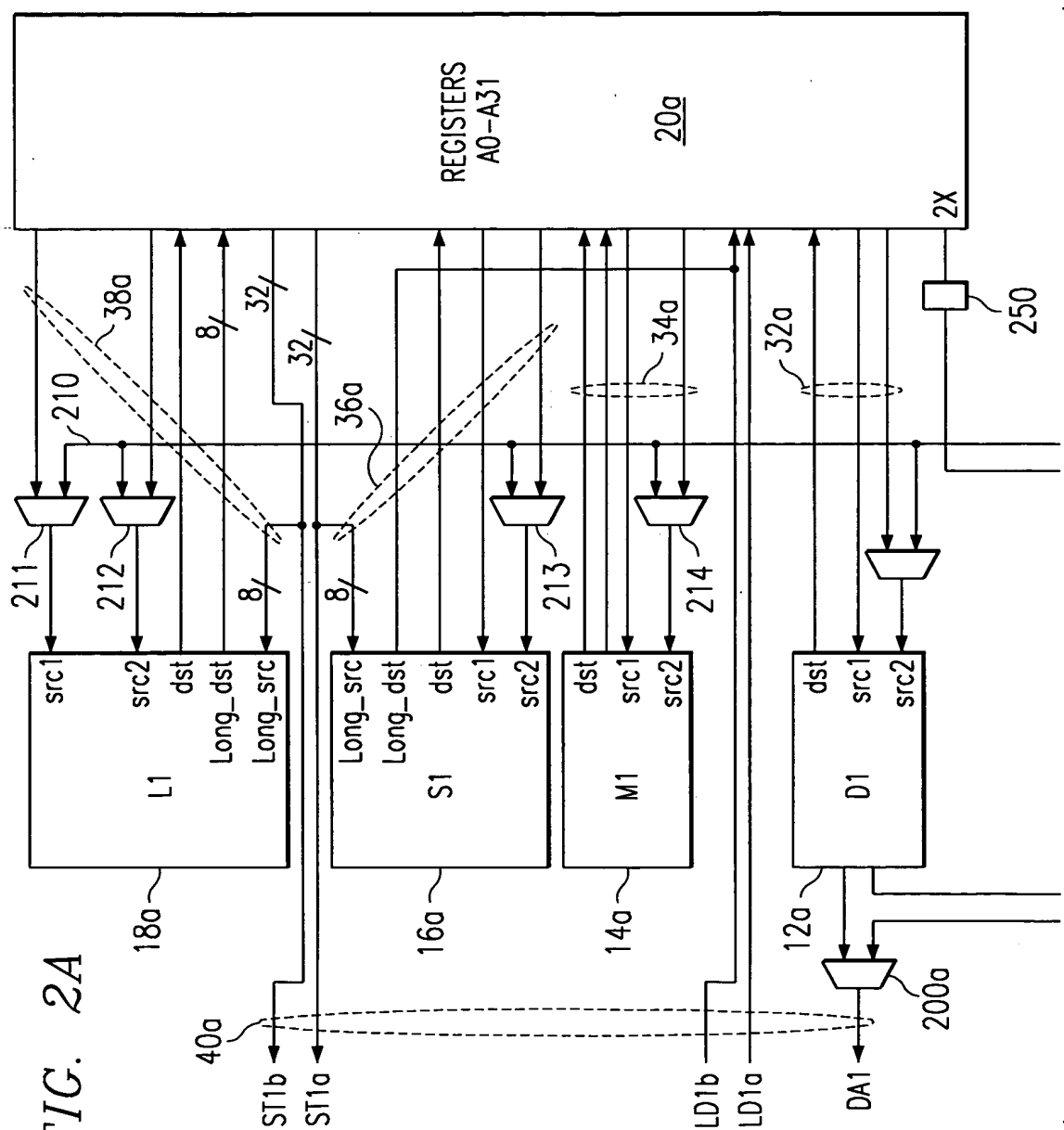


FIG. 1

FIG. 2A



FROM FIG. 2A

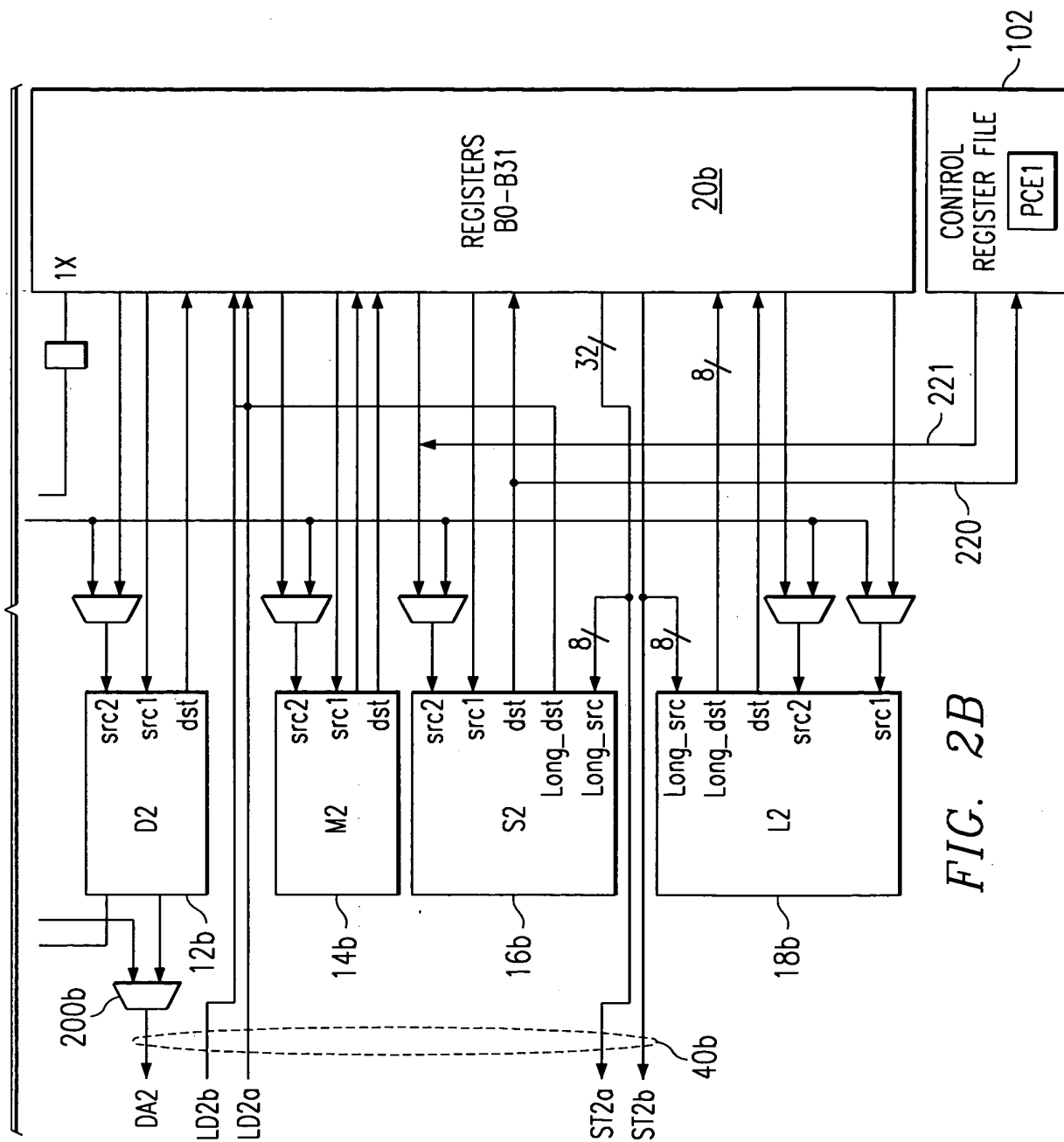
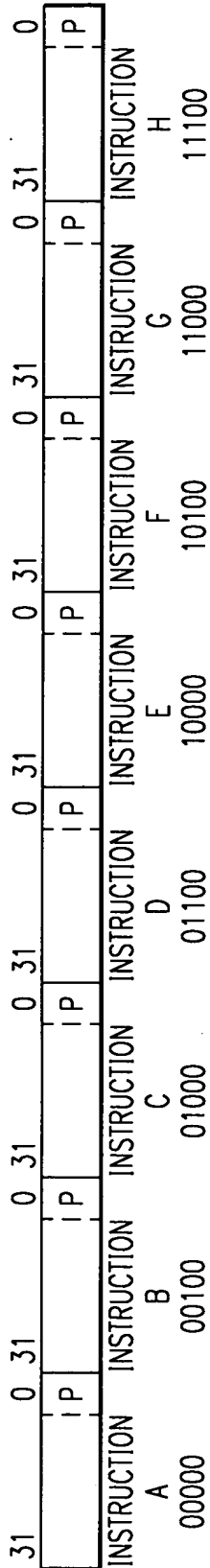


FIG. 2B



LSBs OF
THE BYTE
ADDRESS

FIG. 3A

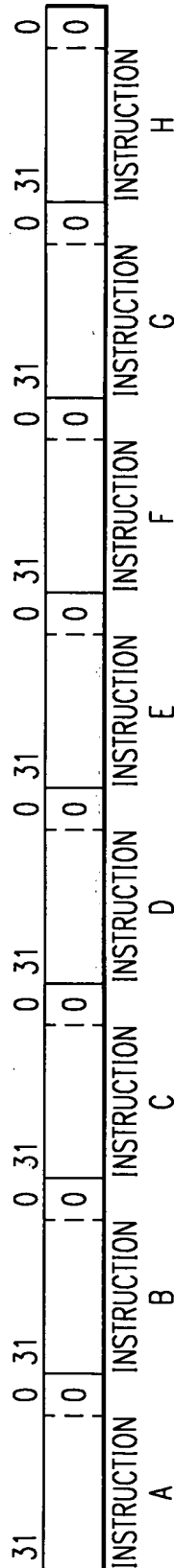


FIG. 3B

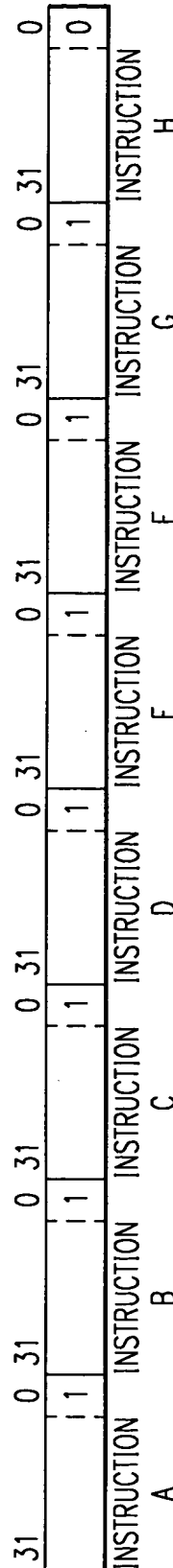


FIG. 3C

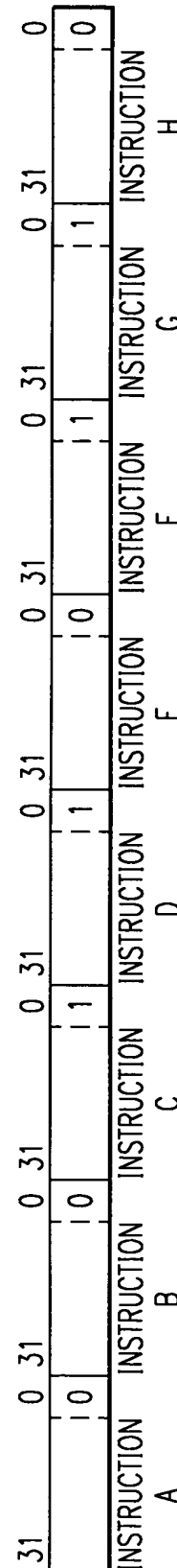


FIG. 3D

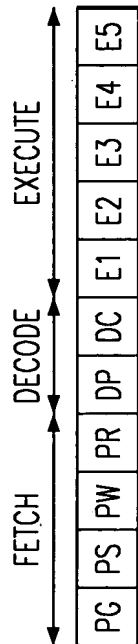


FIG. 4A

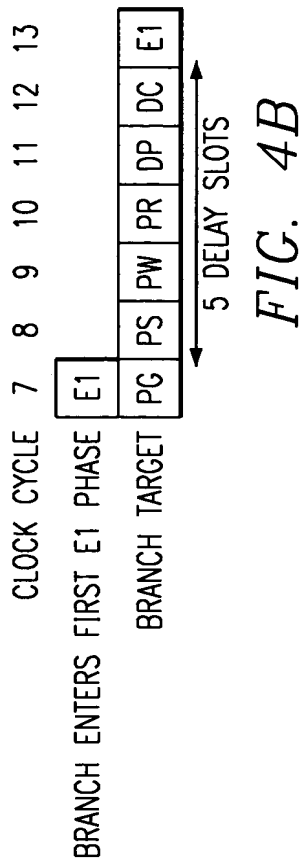
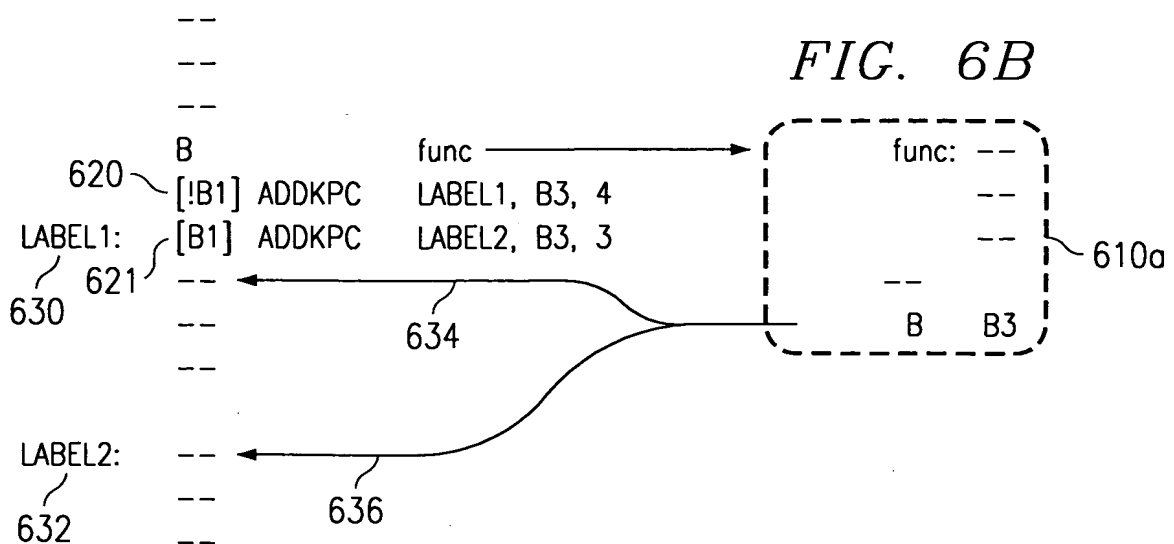
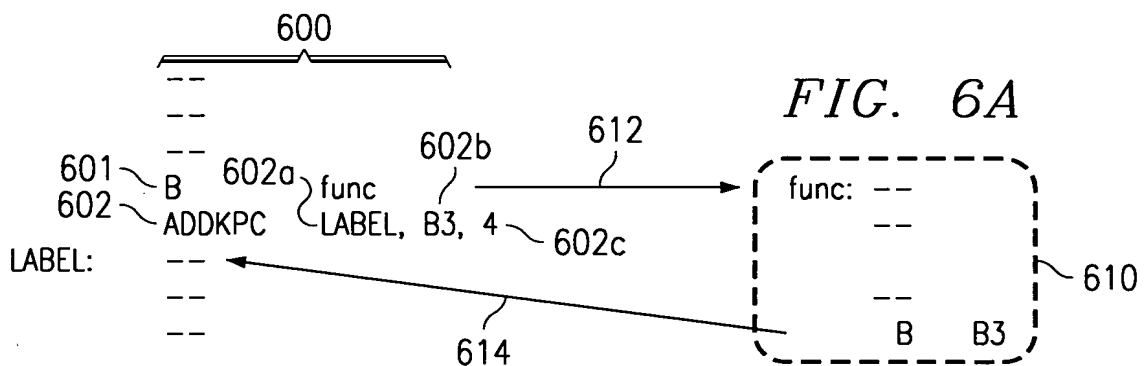
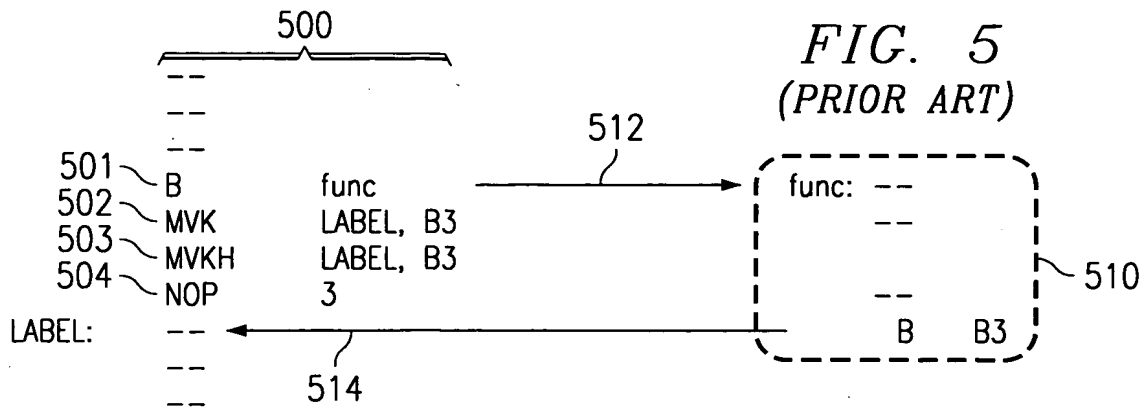


FIG. 4B

		CLOCK CYCLE																						
FETCH PACKET	EXECUTE PACKET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
n	k	PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5												
n	k+1						DP	DC	E1	E2	E3	E4	E5											
n	k+2							DP	DC	E1	E2	E3	E4	E5										
n+1	k+3		PG	PS	PW	PR	PR	PR	DP	DC	E1	E2	E3	E4	E5									
n+2	k+4			PG	PS	PW	PW	PW	PR	DP	DC	E1	E2	E3	E4	E5								
n+3	k+5				PG	PS	PS	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5							
n+4	k+6					PG	PG	PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5						
n+5	k+7								PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5					
n+6	k+8									PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5				
											PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5			
												PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5		

FIG. 4C



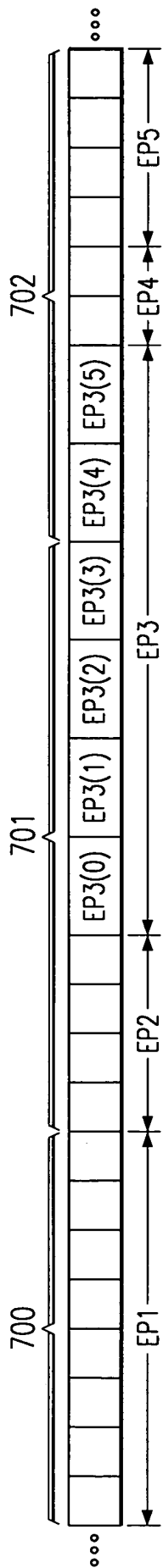


FIG. 7

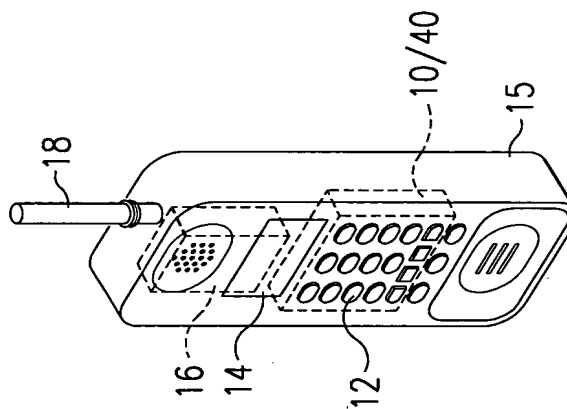


FIG. 11



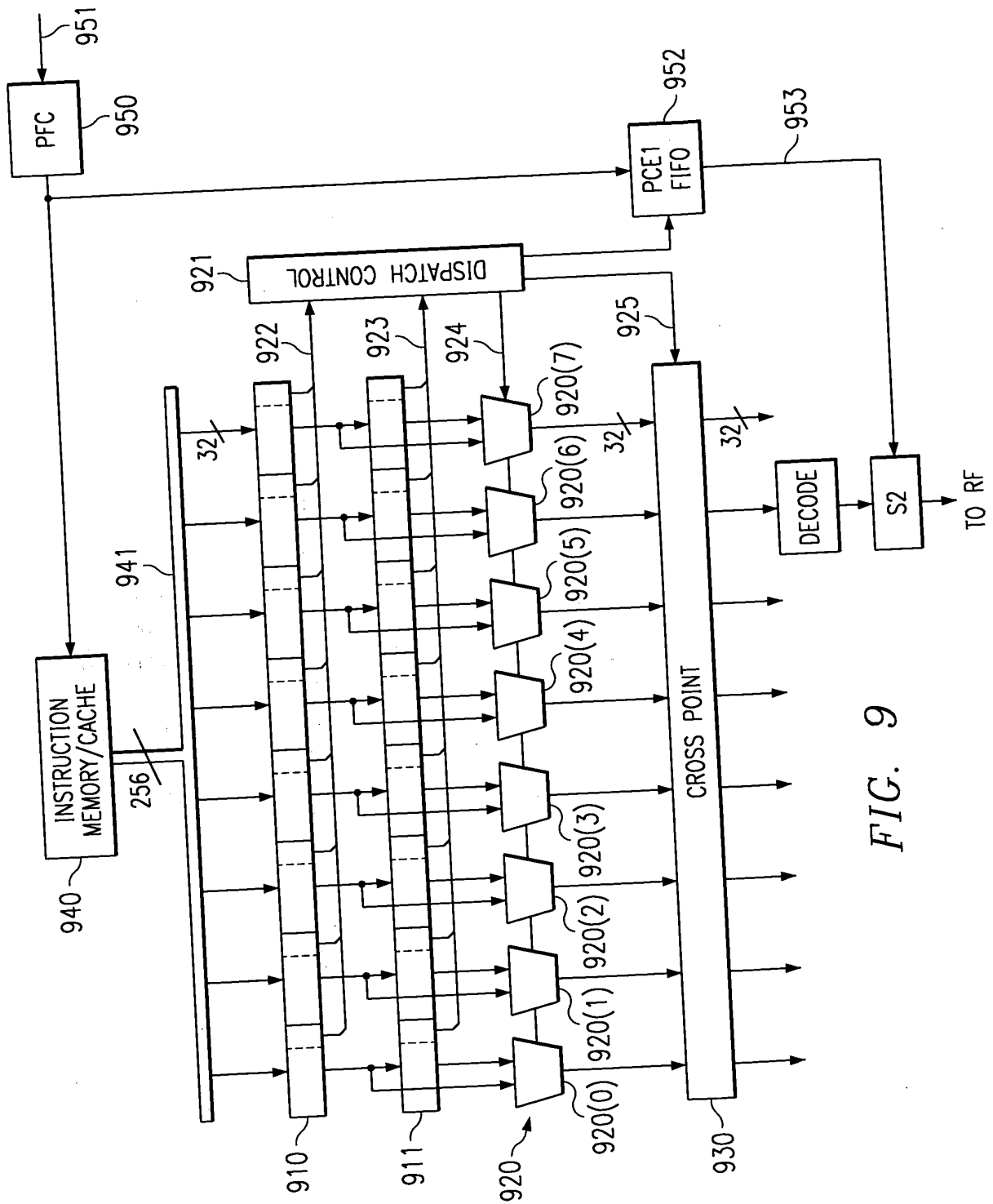


FIG. 9

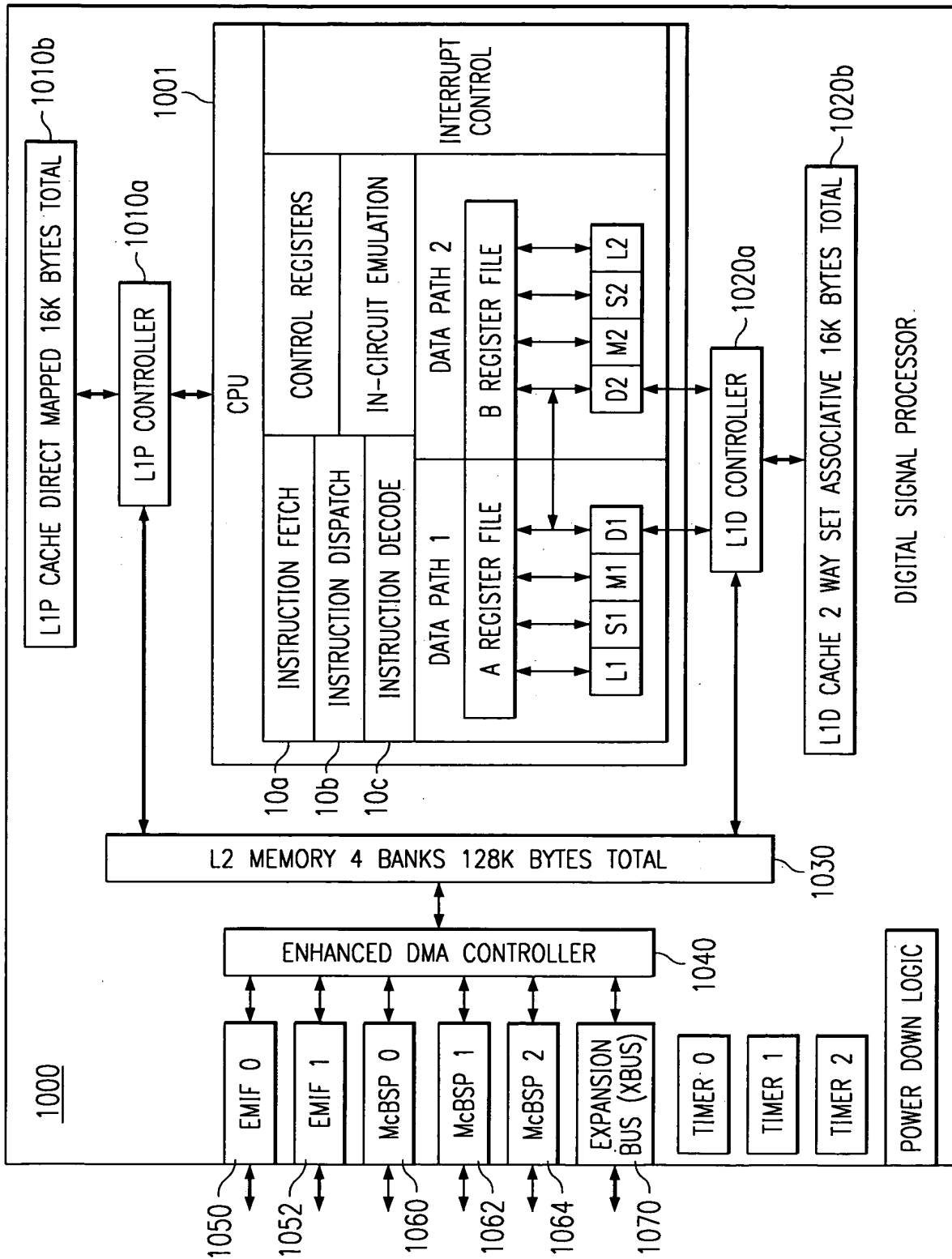


FIG. 10